

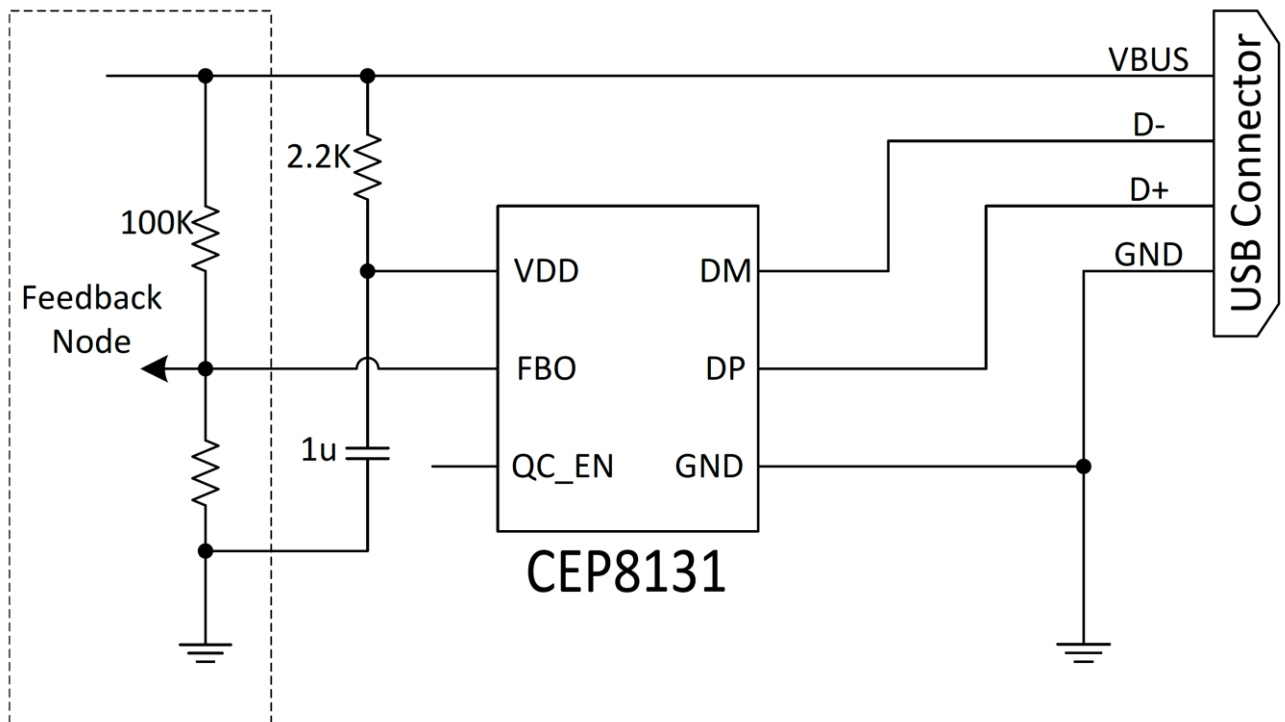
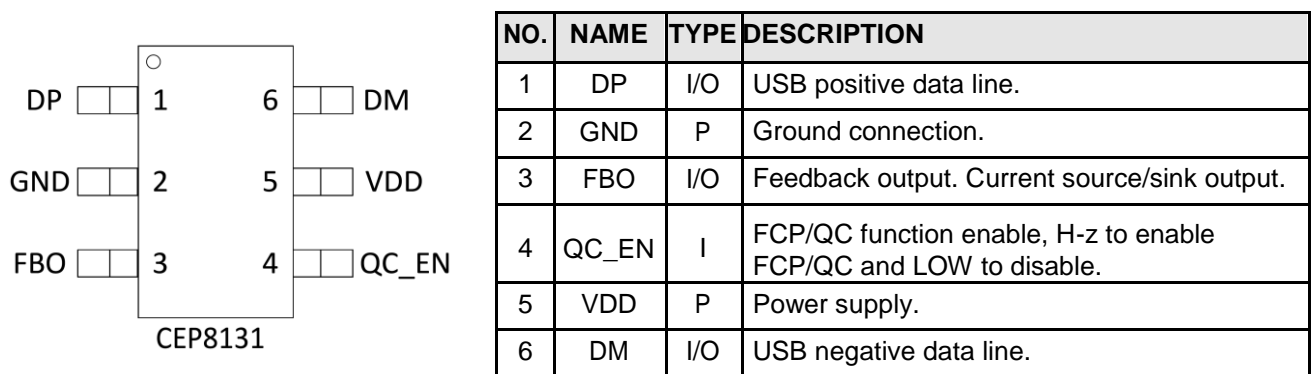
■ FEATURES

- Support HiSilicon Fast Charge Protocol (FCP)
 - Support Samsung Adaptive Fast Charging (AFC)
 - Support Qualcomm Quick Charging 3.0/2.0 (QC3.0/QC2.0) Protocol
 - Support USB DCP applying 2.7V on DP and DM line, output Current up to 2.4A for **Apple** Device
 - Meets Battery Charging Specification **BC 1.2** for DCP
- Meets Chinese Telecommunication Industrial Standard YD/T 1591-2009
 - Automatic Selection of D+/D- mode for an attached device
 - Power Consumption below 1mW at 5V output
 - SOT23-6 Package

■ APPLICATIONS

- Adapter
 - Car Charger
- USB Power Output Ports
 - Power Bank

■ PACKAGE and SIMPLIFIED APPLICATION DIAGRAM



■ GENERAL DESCRIPTION

CEP8131 is a low-cost USB Dedicated Fast Charging Port Controller which is fully compatible with BC1.2 and other non BC1.2 standards like YD/T 1591-2009 Apple & Samsung Charging Spec, HiSilicon Fast Charge Protocol, Qualcomm Quick Charging 3.0/2.0.

CEP8131 automatically detect whether a

connected Power Device (PD) is Quick Charge 2.0/3.0 or FCP Capable before enabling output voltage adjustment. If a PD not compliant to Quick Charge 2.0/3.0 is detected the CEP8131 disables output voltage adjustment to ensure safe operation with legacy 5V only USB PDs.

The CEP8131 is available in SOT23-6 package.

■ ABSOLUTE MAXIMUM RATINGS(Note 1)

PARAMETER		MIN	MAX	UNIT
Voltage Range (To PGND)	VDD	-0.3	6.5	V
	Others	-0.3	6.5	V
Operating Junction Temperature	T _J	-40	150	°C
Storage Temperature Range	T _{STG}	-65	150	°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

■ ESD RATING

SYMBOL	PARAMETER	VALUE	UNIT
V _{ESD}	Human Body Model (HBM)	±4000	V

■ RECOMMENDED OPERATING CONDICTIONS

PARAMETER		MIN	TYP	MAX	UNIT
VDD	Input Supply Voltage	3.2	5	6.4	V
C _{VDD}	Input Capacitance	0.47			μF
T _A	Operation Temperature Range	-40		85	°C

■ ELECTRICAL CHARACTERISTICS

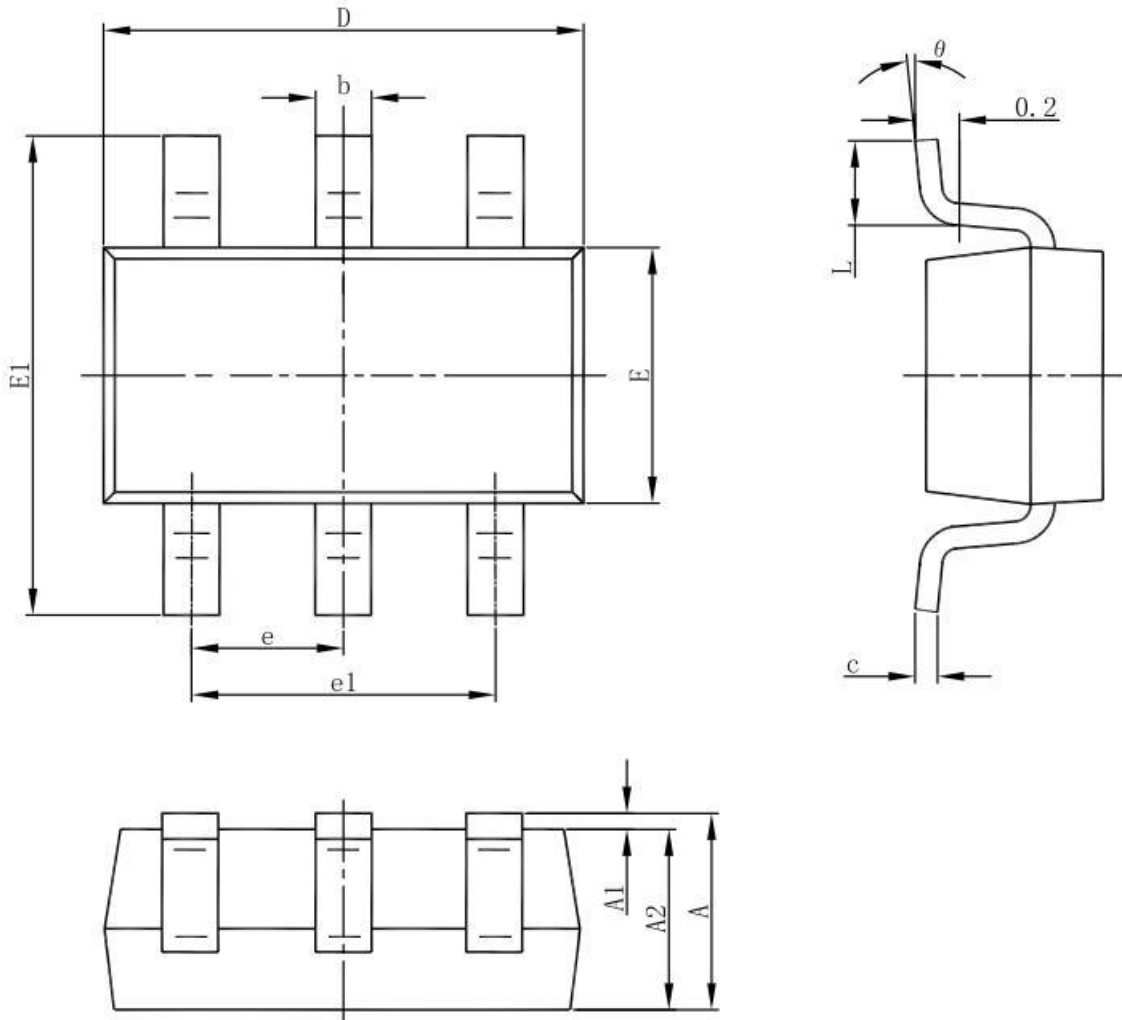
Conditions are T_J=25°C, VDD=5V.

PARAMETER		TEST CONDICTIONS	MIN	TYP	MAX	UNIT
INPUT POWER						
V _{VDD}	VDD Input Voltage Range		3.2		5.5	V
I _{VDD}	VDD Supply Current	VDD=5V		200		uA
V _{VDD(SHUNT)}	VDD Shunt Voltage	I _{VDD} =3.5mA		4.75		V
VDD UVLO Test						
V _{D_(ON)}	VDD (turn on threshold voltage)	V _{VDD} Rising	2.9	3.0	3.1	V
V _{D_(OFF)}	VDD (turn off threshold voltage)	V _{VDD} Falling	2.8	2.9	3.0	V
ΔV _{UVLO}	UVLO Hysteresis	V _{D_(ON)} - V _{D_(OFF)}		0.1		V
High Voltage Dedicated Charging Port (HVDCP)						

V _{DAT(REF)}	Data Detect Voltage		0.25	0.325	0.4	V
V _{SEL(REF)}	Output voltage selection reference		1.8	2	2.2	V
T _{GLITCH(DP)HIGH}	D+ High Glitch Filter Time		1	1.25	1.5	s
T _{GLITCH(DM)LOW}	D- Low Glitch Filter Time			1		ms
T _{GLITCH(V)CHANGE}	Output Voltage Glitch Filter Time		20	40	60	ms
T _{GLITCH(CONT)CHANGE}	Continuous Mode Glitch Filter Time		100	150	200	us
R _{DAT(LKG)}	D+ Leakage Resistance	VDD=3.1-7V, V(D+)=0.5-3.6V, Switch SW1=Off	300	500	800	KΩ
R _{DM(DWN)}	D- Pull-Down Resistance		14.2	19.5	24.5	KΩ
R _{ON(N1)}	Switch SW1 on-resistance	VDD=3.1-7V, V(D+)≤3.6V, IDRAIN=200uA		20	40	Ω
C _{DAT}	Data Line Capacitance				1	nF
V _{TH(PD)}	Output Device Connection Detection threshold		0.25	0.325	0.4	V
T _{DPD}	Output Device connection Detection Glitch Filter Time		120	160	200	ms
ΔI _{T(UP)}	Up Current Step	R _{IREF} =100KΩ		2		uA
ΔI _{T(DO)}	Down Current Step	R _{IREF} =100KΩ		2		uA
T _{DUR(step)}	Duration for current step	QC3.0 mode	80	100	120	us
DCP 1.2V Mode						
V _{DAT(1.2V)}	D+_1.2V/D-_1.2V line output voltage		1.08	1.2	1.32	V
R _{DAT(1.2V)}	D+_1.2V/D-_1.2V line output Impedance			100		KΩ
Apple 2.4A Mode						
V _{DAT(2.7V)}	D+/D- line output voltage		2.57	2.7	2.84	V
R _{DAT(2.7V)}	D+/D- line output Impedance			33.6		KΩ
FCP Mode						
V _{TX-VOH}	D- FCP TX Valid High		2.35		3.6	V
V _{TX-VOL}	D- FCP TX Valid Low				0.3	V
V _{RX-VIH}	D- FCP RX Valid High		1.5		3.6	V
V _{RX-VIL}	D- FCP RX Valid High				1.0	V
R _{PD}	D- Pull-Down Resistance		400	500	600	Ω
T _{UI}	Unit Interval for PHY	F _{CLK} =125KHz	144	160	176	us
T _{RISE}	FCP Pulse Rise Time	10% - 90%		1	2.5	us
T _{FALL}	FCP Pulse Fall Time	90% - 10%		1	2.5	us

■ PACKAGE OUTLINE

SO23-6 PACKAGE OUTLINE AND DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950		0.037	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°