CEP6525

High Precision CC/CV Primary-Side PWM Controller

FEATURES

- **5% Constant Voltage Regulation, 5% Constant Current Regulation at Universal AC input**
- **Primary-side Sensing and Regulation Without TL431 and optocoupler**
- **Programmable CV and CC Regulation**
- **Adjustable Constant Current and Output Power Setting**
- **Built-in Secondary Constant Current Control with Primary Side Feedback**
- **Built-in Adaptive Current Peak Regulation**
- **Built-in Primary winding inductance compensation**
- **Programmable Cable drop Compensation**
- **Power on Soft-start**
- **Built-in Leading Edge Blanking (LEB)**
- **Cycle-by-Cycle Current Limiting**
- **VDD Under Voltage Lockout with Hysteresis(UVLO)**
- **VDD OVP**
- **VDD Clamp**

APPLICATIONS

Low Power AC/DC offline SMPS for

- **Cell Phone Charger**
- **Digital Cameras Charger**
- **Small Power Adaptor**
- **Auxiliary Power for PC, TV etc.**
- **Linear Regulator/RCC Replacement**

GENERAL DESCRIPTION

CEP6525 is a high performance offline PWM Power switch for low power AC/DC charger and adaptor applications. It operates in primary-side sensing and regulation. Consequently, optocoupler and TL431 could be eliminated. Proprietary Constant Voltage (CV) and Constant Current (CC) control is integrated as shown in the figure below. In CC control, the current and output power setting can be adjusted externally by the sense resistor Rs at CS pin. In CV control, multi-mode operations are utilized to achieve high performance and high efficiency. In addition, good load regulation is achieved by the built-in cable drop compensation. Device operates in PFM in CC mode as well at large load condition and it operates in PWM with frequency reduction at light/medium load. CEP6525 offers power on soft start control and protection coverage with auto-recovery features including Cycle-by-Cycle current limiting, VDD OVP, VDD clamp and UVLO.

High precision constant voltage (CV) and constant current (CC) can be achieved by CEP6525.

Typical CC/CV Curve

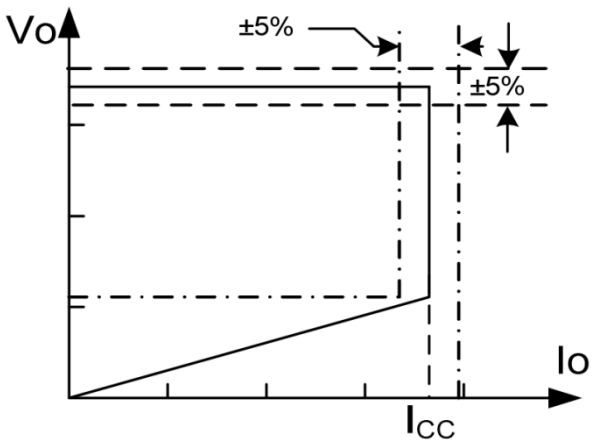
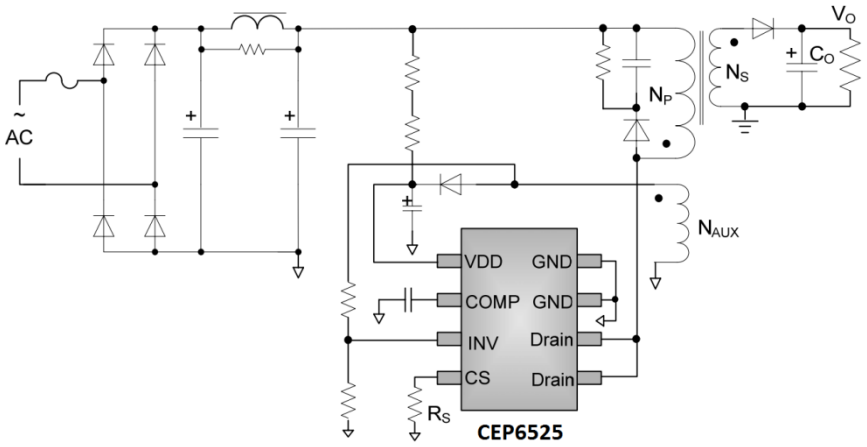


Fig.1. Typical CC/CV Curve

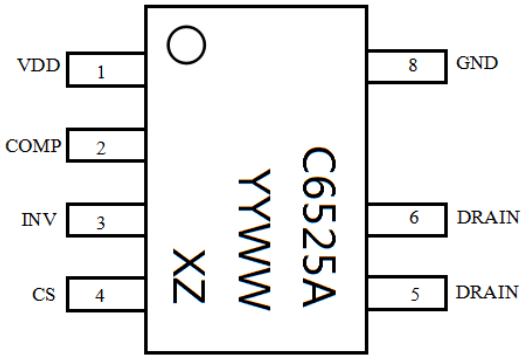
TYPICAL APPLICATION

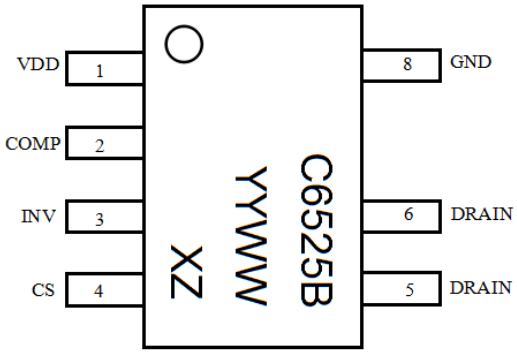


ORDERING INFORMATION

PART NUMBER	Min/Max Storage Temperature	PACKAGE	PINS	PACKING
CEP6525ASP8	-55°C to 150°C	SOP-8	8	TAPE & REEL
CEP6525BSP8	-55°C to 150°C	SOP-8	8	TAPE & REEL
CEP6525ADP8	-55°C to 150°C	DIP-8	8	TUBE

PIN Configuration AND Marking Information





C6525A/C6525B : Product Number
YYWW : Date Code
XZ : Factory code

PIN DESCRIPTIONS

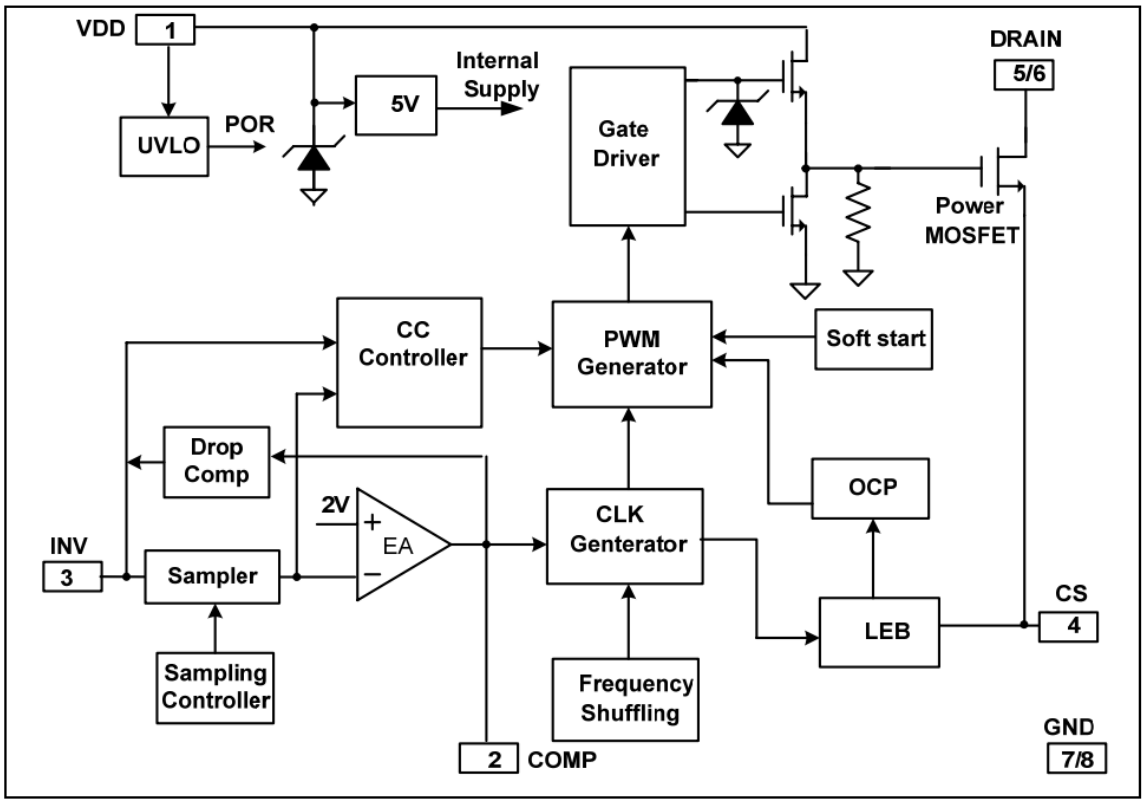
Pin No.	NAME	Description
1	VDD	Power Supply
2	COMP	Input Pin. Loop Compensation for CV Stability
3	INV	Input Pin. The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage. PWM duty cycle is determined by EA output and current sense signal at pin 4.
4	CS	Input Pin. Current sense.
5/6	DRAIN	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer
7/8	GND	Ground

OUTPUT POWER TABLE

Product	230VAC±15%	85-264VAC
CEP6525ASP8	15W	12W
CEP6525BSP8	11W	8W
CEP6525ADP8	20W	15W

Note: Maximum practical continuous power in an Adapter design with sufficient drain pattern as a heat sink, at 50℃ ambient.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Drain Voltage (off state)	-0.3 to Bvdss	V
VDD Voltage	-0.3 to VDD_clamp	V
Continuous Current	10	mA
COMP Voltage	-0.3 to 7	V
CS Input Voltage	-0.3 to 7	V
INV Input Voltage	-0.3 to 7	V
Max Operating Junction Temperature TJ	150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

CEP6525ASP8 , CEP6525ADP8 (TA = 25℃ , VDD=VDDG=16V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
Isb	Standby Current	VDD=13V		5	20	uA
IDD	Operation Current	Operation supply current INV=2V, CS=0V, VDD=VDDG=18V		2	3	mA
UVLO(ON)	VDD Under Voltage Lockout Enter	VDD falling	8.2	9.0	10.5	V
UVLO(OFF)	VDD Under Voltage Lockout Exit	VDD rising	13.5	14.8	16.0	V
VDD_clamp	Maximum VDD operation voltage	IDD=10mA	27	28	30	V
OVP	Over voltage protection Threshold	Ramp VDD until gate shut down	26	27.5	29	V
Current Sense Input Section						
TLEB	LEB time			625		nS
Vth_oc	Over current threshold		880	910	940	mV
Td_oc	OCP Propagation delay			110		nS
Z_{SENSE}_IN	Input Impedance		50			KΩ
T_ss	Soft start time			17		mS
Frequency Section						
Freq_Max *Note 1	IC Maximum frequency		55	60	65	KHz
Freq_Nom	System Nominal switch frequency			50		KHz
Freq_startup		NV=0V, Comp=5V		14		KHz
△ f/Freq	Frequency shuffling range			6		%
Error Amplifier section						
Vref_EA	Reference voltage for EA		1.96	2	2.04	V
Gain	DC gain of EA			60		dB
I_COMP_MAX	Max. Cable compensation current	INV=2V, Comp=0V		37.5		uA
Power MOSFET Section						
BVdss	MOSFET Drain-Source Breakdown Voltage		650			V
Rdson	On Resistance	Static, Id=1.0A		3.8		Ω

Note:

1. Freq_Max indicates IC internal maximum clock frequency. In system application, the maximum operation frequency of 60Khz nominal occurs at maximum output power or the transition point from CV to CC.

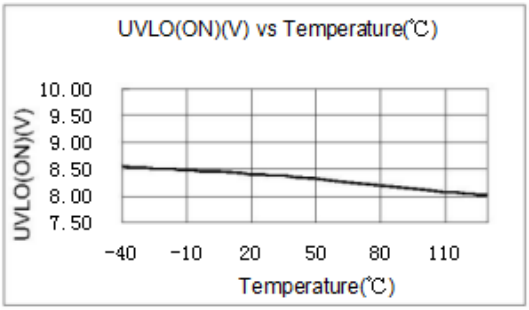
CEP6525BSP8 (TA = 25℃ , VDD=VDDG=16V, if not otherwise noted)

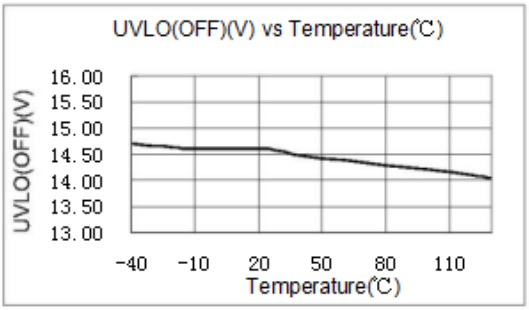
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
Isb	Standby Current	VDD=13V		5	20	uA
IDD	Operation Current	Operation supply current INV=2V, CS=0V, VDD=VDDG=18V		2	3	mA
UVLO(ON)	VDD Under Voltage Lockout Enter	VDD falling	8.2	9.0	10.5	V
UVLO(OFF)	VDD Under Voltage Lockout Exit	VDD rising	13.5	14.8	16.0	V
VDD_clamp	Maximum VDD operation voltage	IDD=10mA	27	28	30	V
OVP	Over voltage protection Threshold	Ramp VDD until gate shut down	26	27.5	29	V
Current Sense Input Section						
TLEB	LEB time			625		nS
Vth_oc	Over current threshold		880	910	940	mV
Td_oc	OCP Propagation delay			110		nS
Z_{SENSE}_IN	Input Impedance		50			KΩ
T_ss	Soft start time			17		mS
Frequency Section						
Freq_Max *Note 1	IC Maximum frequency		55	60	65	KHz
Freq_Nom	System Nominal switch frequency			50		KHz
Freq_startup		NV=0V, Comp=5V		14		KHz
△ f/Freq	Frequency shuffling range			6		%
Error Amplifier section						
Vref_EA	Reference voltage for EA		1.96	2	2.04	V
Gain	DC gain of EA			60		dB
I_COMP_MAX	Max. Cable compensation current	INV=2V, Comp=0V		37.5		uA
Power MOSFET Section						
BVdss	MOSFET Drain-Source Breakdown Voltage		650			V
Rdson	On Resistance	Static, Id=1.0A		4.8		Ω

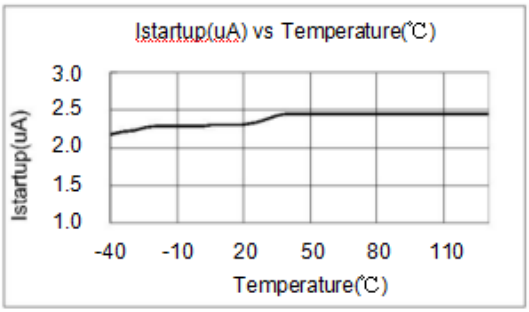
Note:

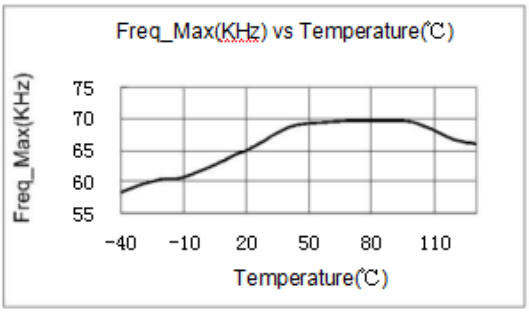
1. Freq_Max indicates IC internal maximum clock frequency. In system application, the maximum operation frequency of 60Khz nominal occurs at maximum output power or the transition point from CV to CC.

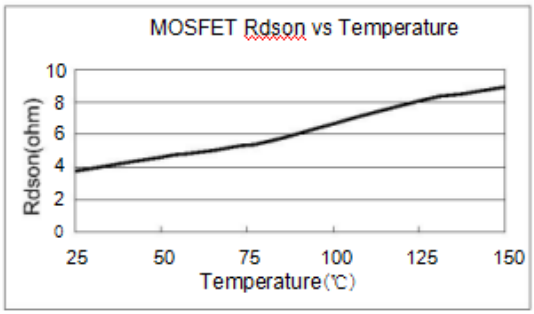
CHARACTERIZATION PLOTS











OPERATION DESCRIPTION

CEP6525 is a cost effective PWM power switch optimized for off-line low power AC/DC applications including battery chargers and adaptors. It operates in primary side sensing and regulation, thus opto-coupler and TL431 are not required. Proprietary built-in CV and CC control can achieve high precision CC/CV control meeting most adaptor and charger application requirements.

➢ Startup Current and Start up Control

Startup current of CEP6525 is designed to be very low so that VDD could be charged up above UVLO threshold and starts up quickly. A large value startup resistor can therefore be used to minimize the power loss in application.

➢ Operating Current

The Operating current of CEP6525 is as low as 2.5mA. Good efficiency is achieved with the low operating current together with 'Muti-mode' control features.

➢ Soft Start

CEP6525 features an internal soft start to minimize the component electrical over-stress during power on startup. As soon as VDD reaches UVLO (OFF), the control algorithm will ramp peak current voltage threshold gradually from nearly zero to normal setting of 0.90V. Every restart is a soft start.

➢ CC/CV Operation

CEP6525 is designed to produce good CC/CV control characteristic as shown in the Fig. 1. In charger applications, a discharged battery charging starts in the CC portion of the curve until it is nearly full charged and smoothly switches to operate in CV portion of the curve. In an AC/DC adapter, the normal operation occurs only on the CV portion of the curve. The CC portion provides output current limiting. In CV operation, the output voltage is regulated through the primary side control. In CC operation mode, CEP6525 will regulate the output current constant regardless of the output voltage drop.

➢ Principle of Operation

To support CEP6525 proprietary CC/CV control, system needs to be designed in DCM mode for flyback system (Refer to Typical Application Diagram on page1). In the DCM flyback converter, the output voltage can be sensed via the auxiliary winding.During MOSFET turn-on time, the load current is supplied from the output filter capacitor. The current in the primary winding ramps up. When MOSFET turns off, the primary current transfers to the secondary at the amplitude of

$$I_S = \frac{N_P}{N_S} \times I_P \qquad (1)$$

The auxiliary voltage reflects the output voltage as shown in fig.2 and it is given by

$$V_{AUX} = \frac{N_{AUX}}{N_S} \times (V_O + \Delta V) \qquad (2)$$

Where ΔV indicates the drop voltage of the output Diode.

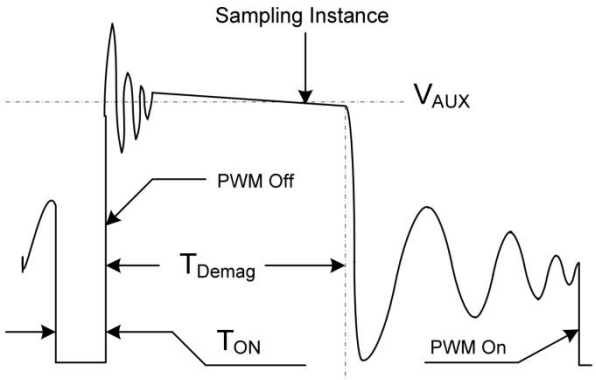


Fig.2. Auxiliary voltage waveform

Via a resistor divider connected between the auxiliary winding and INV (pin 3), the auxiliary voltage is sampled at the end of the de-magnetization and it is hold until the next sampling. The sampled voltage is compared with Vref (2.0V) and the error is amplified. The error amplifier output COMP reflects the load condition and controls the PWM switching frequency to regulate the output voltage, thus constant output voltage can be achieved. When sampled voltage is below Vref and the error amplifier output COMP reaches its maximum, the switching frequency is controlled by the sampled voltage thus the output voltage to regulate the output current, thus the constant output current can be achieved.

➢ Adjustable CC point and Output Power

In CEP6525, the CC point and maximumoutput power can be externally adjusted by external current sense resistor Rs at CS pin as illustrated in Typical Application Diagram. The output power is adjusted through CC point change. The larger Rs, the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Fig.3.

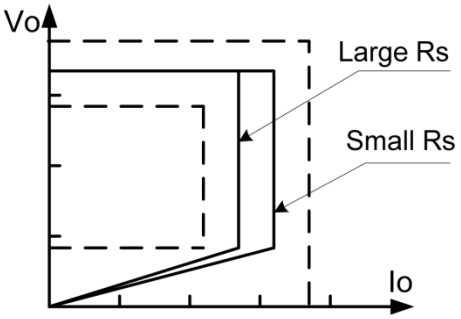


Fig.3 Adjustable output power by changing Rs

➢ **Operation switching frequency**

The switching frequency of CEP6525 is adaptively controlled according to the load conditions and the operation modes. No external frequency setting components are required. The operation switching frequency at maximum output power is set to 60K Hz internally. For flyback operating in DCM, The maximum output power is given by

$$P_{O_{MAX}} = \frac{1}{2} L_P F_{SW} I_P^2 \qquad (3)$$

Where Lp indicate the inductance of primary winding and Ip is the peak current of primary winding.

Refer to the equation 3, the change of the primary winding inductance results in the change of the maximum output power and the constant output current in CC mode. To compensate the change from variations of primary winding inductance, the switching frequency is locked by an internal loop such that the switching frequency is

$$F_{SW} = \frac{1}{2T_{Demag}} \qquad (4)$$

Since T_{Demag} is inversely proportional to the inductance, as a result, the product Lp and fsw is constant, thus the maximum output power and constant current in CC mode will not change as primary winding inductance changes. Up to +/-10% variation of the primary winding inductance can be compensated.

➢ **Frequency shuffling for EMI improvement**

The frequency shuffling (switching frequency modulation) is implemented in CEP6525. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

➢ **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in CEP6525 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state so that the external RC filtering on sense input is no longer needed. The PWM duty cycle is determined by the current sense input voltage and the EA output voltage.

➢ **Gate Drive**

The internal power MOSFET in CEP6525 is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive compromises EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength control.

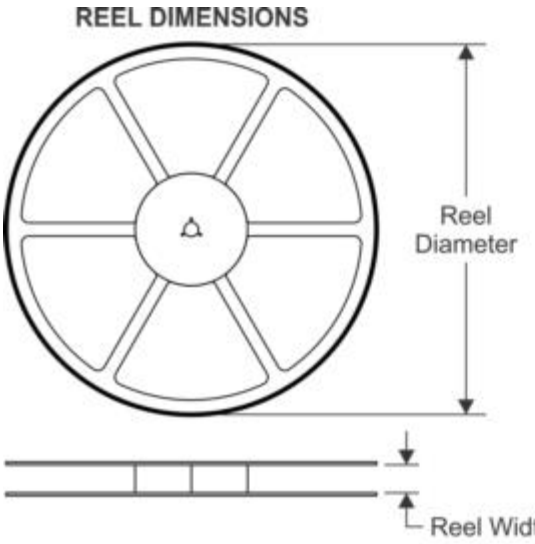
➢ **Programmable Cable drop Compensation**

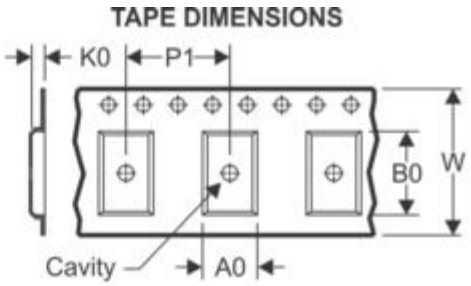
In CEP6525, cable drop compensation is implemented to achieve good load regulation. An offset voltage is generated at INV by an internal current flowing into the resister divider. The current is inversely proportional to the voltage across pin COMP, as a result, it is inversely proportional to the output load current, thus the drop due to the cable loss can be compensated. As the load current decreases from full-load to no-load, the offset voltage at INV will increase. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used.

➢ **Protection Control**

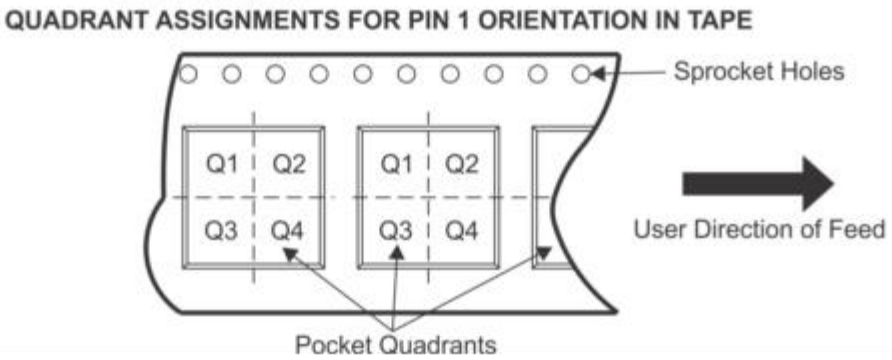
Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), VDD clamp, Power on Soft Start, and Under Voltage Lockout on VDD (UVLO). VDD is supplied by transformer auxiliary winding output. The output of CEP6525 is shut down when VDD drops below UVLO (ON) limit and Switcher enters power on start-up sequence thereafter.

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

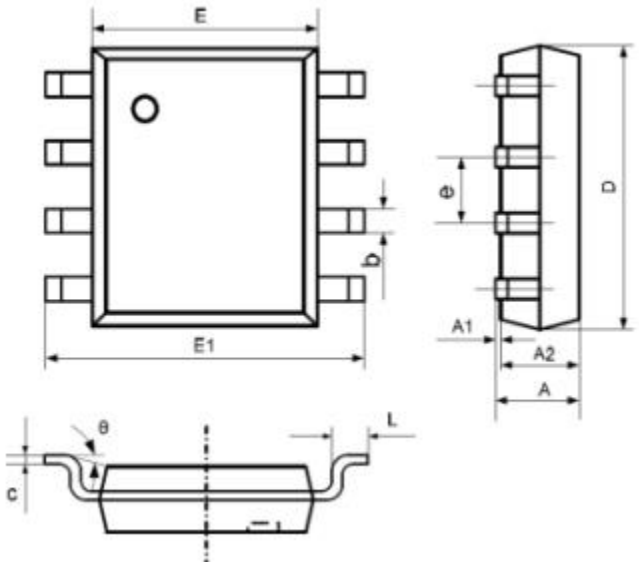


***All dimensions are nominal**

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CEP6525ASP8	SOP-8	C6525	8	2500	330.0	12.8	6.4	5.2	2.5	8.0	12.0	Q1
CEP6525BSP8	SOP-8	C6525	8	2500	330.0	12.8	6.4	5.2	2.5	8.0	12.0	Q1

PACKAGE OUTLINE

SOP-8 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.700	0.053	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°